A HIGHLY MINIATURIZED RECEIVER FRONT-END HYBRID IC USING ON-CHIP HIGH-DIELECTRIC CONSTANT CAPACITORS FOR MOBILE COMMUNICATION EQUIPMENT

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ABSTRACT

A highly miniaturized and low power consumption receiver front-end hybrid IC(HIC) including input matching circuits for 880MHz bands using on-chip high-dielectric constant (ε_r) capacitors has been newly developed. The HIC is composed of a GaAs IC chip and a ceramic substrate with spiral inductors on its surface. The HIC showed conversion gain of 20.2dB and noise figure of 4.2dB at supply voltage of 2.7V and dissipation current of 3.7mA. The HIC measures only 5.0mm×5.0mm×1.0mm.

INTRODUCTION

In order to miniaturize mobile communication equipment, integration of circuits and low power consumption are the most effective method to realize the objective. Although several works have been reported on miniaturization and low power operation, most of them still needed external chip components for matching circuits or a.c. grounding[1]-[3]. To accomplish the objective, we have already reported on the HIC including matching circuits on the ceramic substrate by applying the flip-chip bonding technology to the GaAs front-end IC[4], however, relatively large occupation area of chip capacitors on the ceramic substrate was an obstacle to further miniaturization and reduction in cost.

This paper describes the development of a highly miniaturized receiver front-end HIC using high-ε_r on-chip capacitors and its superior RF performance at low power consumption.

HIC DESIGN

A. Technologies for HIC

In order to achieve miniaturization and low power consumption, the following new technologies were developed and applied to the HIC;

(1) Flip-chip bonding using micro bump bonding (MBB) technology,
(2) Intermediate tuned circuits for the GaAs IC,
(3) Integrating capacitors on the GaAs IC chip by using high-ε_r $SrTiO_3$ thin film process,
(4) Adopting LDD self-aligned buried p-layer MESFETs (BP-MESFETs) with 0.5μm of refractory metal gate.

B. Flip-Chip Bonding

Figure 1 shows the schematic cross-sectional view of the fabricated HIC. The flip-chip bonding using the MBB technology[8] was applied to the HIC to minimize the parasitic elements and bonding pads area.

After the IC chip was connected to the ceramic substrate by Au micro bumps of 20μm in diameter, a gap between the face of the IC chip and that of the ceramic substrate was filled with insulating resin. Only 50μm × 50μm of openings in the bonding pads on the IC chip were required for the MBB. The height of the micro bump was 2-3μm, and the influence of the micro bump was confirmed to be negligible up to 10GHz.

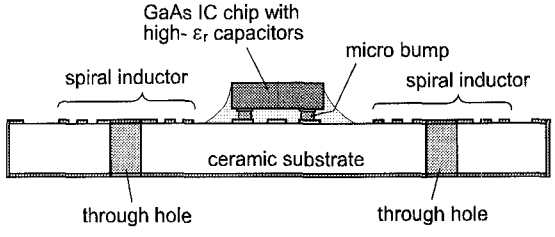

Fig.1 Schematic cross-sectional view of the HIC.

C. GaAs Front-End IC

Figure 2 shows an equivalent circuit diagram of the HIC. The HIC is composed of a receiver front-end GaAs IC chip, input matching circuits and intermediate tuned circuits[3][4]. The GaAs IC contains an LNA, an LO amplifier and a single-ended down-conversion mixer.

A self-biased common source dual-gate MESFETs were adopted for those circuits because of its simple configuration for high yield, low dissipation current, and good RF characteristics, especially in isolations. High isolations were realized by a.c. grounding the 2nd gates of the FETs for the LNA and LO amplifier.

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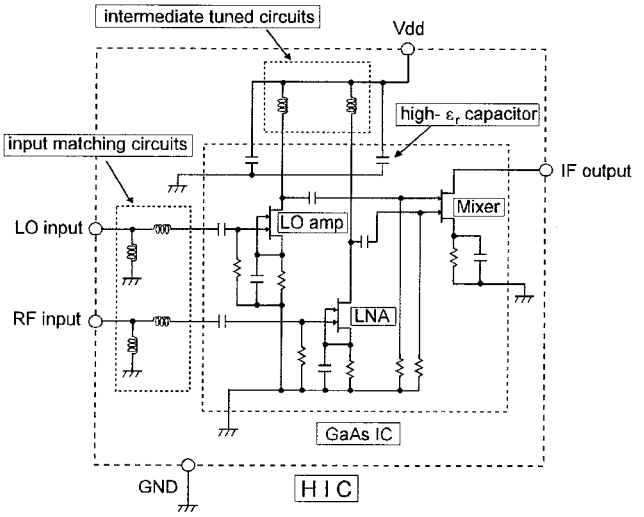

Fig.2 Equivalent circuit diagram of the HIC. The HIC is composed of GaAs IC, input matching circuits and intermediate tuned circuits.

A high image rejection ratio was realized by adopting both the narrow-band RF input matching circuit and the intermediate tuned circuit between the LNA and the mixer. The intermediate tuned circuit was composed of the inductance of the external inductor, the input capacitance of the mixer, and the output capacitance of the LNA. The high image rejection ratio made it possible to eliminate a band-pass filter between the LNA and the mixer. The intermediate tuned circuit was also applied to the interconnection between the LO amplifier and the mixer to lower the LO input power. As a result, -20dBm of LO input power was enough to operate the HIC.

The input matching circuits for the LNA and LO amplifier were constructed by the series and shunt inductors, because this topology of circuit could offer the smallest occupation area, high image rejection ratio and good tolerance to fluctuation of line width.

PROCESS TECHNOLOGY

A. High-ε_r Capacitor

To highly miniaturize the ceramic substrate, bypass capacitors for the amplifiers and the mixer and for the intermediate tuned circuits, and input dc cut-out capacitors were integrated on the GaAs IC chip by using high-ε_r $SrTiO_3$ thin film. The $SrTiO_3$ thin film was deposited on the Pt electrodes by the low-temperature RF sputtered process technology[7]. Film deposition temperature was 300C° and thickness of film was 300nm. ε_r of 120, leakage current density under 10^{-6}A/cm^2 at 1MV/cm, and breakdown voltage over 30V were obtained. By integrating those capacitors on the IC chip, only spiral inductors for the input matching circuits and the intermediate tuned circuits were left to the surface of the ceramic substrate.

B. LDD BP-MESFETs

The GaAs BP-MESFETs were fabricated by using the buried p-layer(BP) asymmetric self-aligned LDD (Lightly Doped Drain) process using WSi as gate[5][6]. An asymmetric LDD structure was adopted to improve break-down voltage between the second gate and drain. A buried p-layer was formed by a selective ion implantation of Mg^+ to suppress the short channel effect. Gate lengths were 0.5μm each. Schematic cross-sectional view of the LDD BP-MESFET is shown in Fig.3.

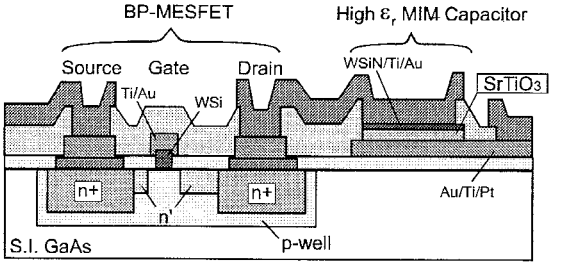

Fig.3 Schematic cross-sectional view of the LDD BP-MESFET and high-ε_r capacitor.

The LDD BP-MESFET was designed to have high k-value and low drain conductance for excellent RF performance at low power consumption. By optimizing the distance between the gate metal and the drain n^+ region, the fabricated BP-MESFETs delivered k-value of 208mA/V^{2}mm and drain conductance of 0.55mS/mm for -1.0V of threshold voltage. Figure 4 shows micro-photograph of the fabricated GaAs front-end IC chip.

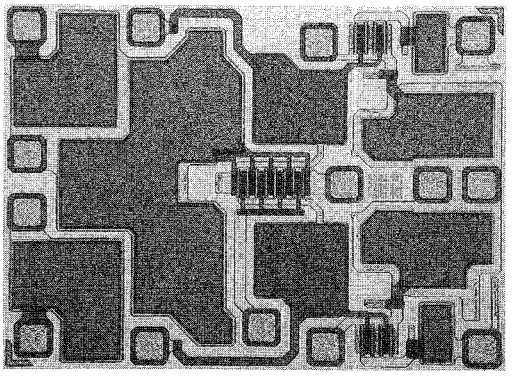

Fig.4 Micro-photograph of the GaAs IC chip. The chip measures 0.8mm × 1.0mm.

C. Fabrication of HIC

By adopting those technologies mentioned above, the fabricated HIC was miniaturized to 5.0mm × 5.0mm × 1.0mm. Top view of the fabricated HIC is shown in Fig.5. It is recognized from this photograph that only spiral inductors for matching and intermediate tuned circuits are left to the surface of the ceramic substrate. Spiral inductors were fabricated by thin metal film process which enabled 30μm of line width within ±10% of fluctuation.

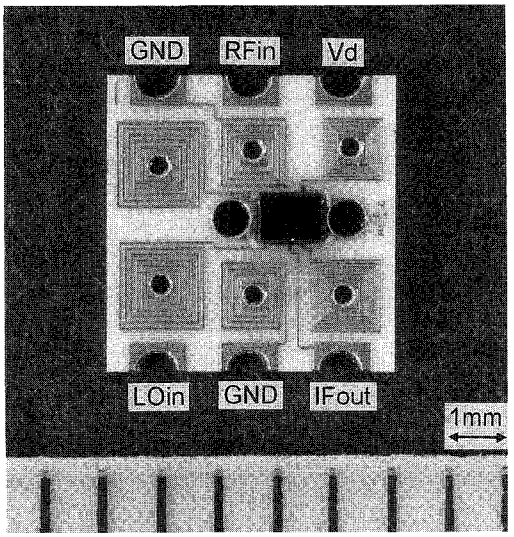

Fig.5 Micro-photograph of the fabricated HIC. The HIC measures 5.0mm×5.0mm×1.0mm.

RF PERFORMANCE

Owing to the technologies applied to the HIC, the fabricated HIC delivered high RF performance with very low power consumption.

LO input power dependency of the conversion gain, noise figure, and IM3 are shown in Fig.6. It is seen from this figure that conversion gain of 20.2dB, noise figure of 4.2dB and IM3 of -34.5dBc are obtained with LO input power of -20dBm. The relatively small LO input power was realized by the intermediate tuned circuit for the LO amplifier.

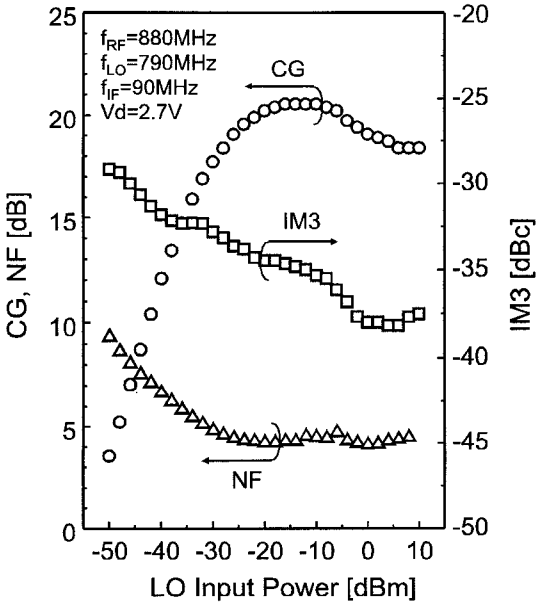

Fig.6 RF performance of the fabricated HIC as a function of LO input power.

Figure 7 indicates Pin-Pout linearity of the fabricated HIC. The 3rd order output intercept point (IP3out) of -2.8dBm is obtained at supply voltage of 2.7V and dissipation current of 3.7mA.

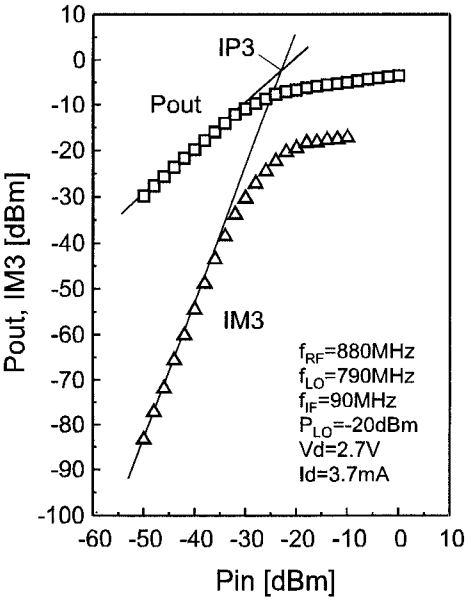

Fig.7 Pin-Pout linearity of the fabricated HIC.

Owing to the low knee-voltage of the fabricated LDD BP-MESFETs, conversion gain, noise figure and IM3 held out to about 2.0V of supply voltage. Dependencies of supply voltages are shown in Fig.8.

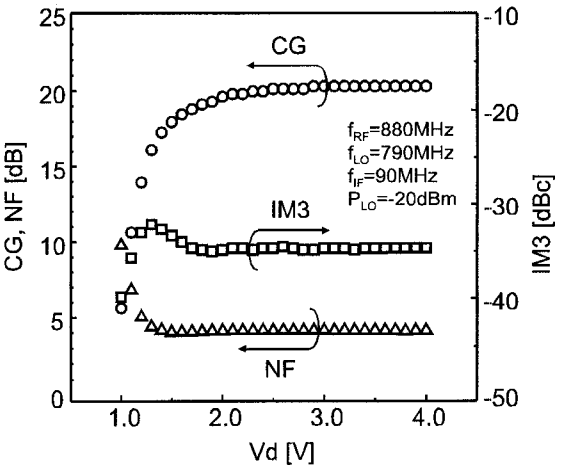

Fig.8 RF performance of the fabricated HIC as a function of supply voltages.

Frequency responses of the HIC is shown in Fig.9. It is seen from this figure that conversion gain of over 17dB, image rejection ratio of over 10dB and noise figure of under 5.0dB are well achieved within ±40MHz of wide frequency range from the center frequency.

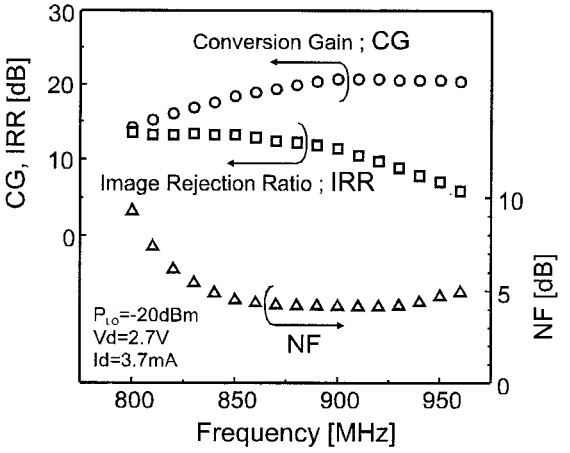

Fig.9 Frequency responses of the fabricated HIC.

By the a.c. grounding of the second gates of the dual-gate FETs for the LNA and LO amplifier, high isolations between LO and RF ports are maintained as shown in Fig.10. Over 15dB of isolations are obtained between these two ports.

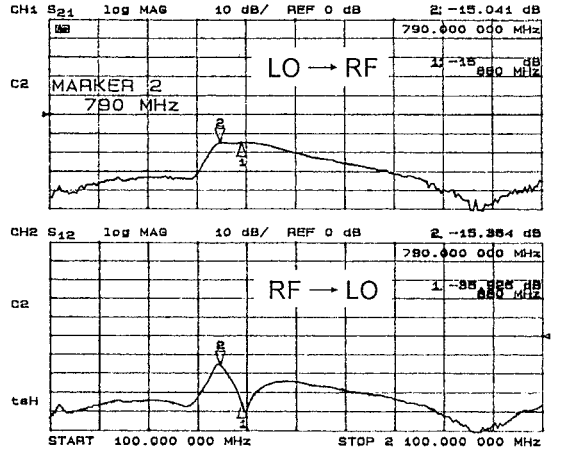

Fig.10 Isolation characteristics of the HIC

Performance of the fabricated HIC at 880MHz bands are summarized in table1.

Table 1 Performance of the fabricated HIC.

Size	5.0mmx5.0mmx1.0mm
Supply Voltage	2.7V
Dissipation Current	3.7mA
Conversion Gain	20.2dB
NF	4.2dB
IP_3 (output)	-2.8dBm
LO to RF Isolation	15dB
Image Rejection Ratio	12dB
Frequency Bands	880MHz

CONCLUSIONS

A highly miniaturized receiver front-end HIC using on-chip high dielectric constant capacitors and 0.5μm-gate LDD BP-MESFETs for 880MHz bands mobile communication equipment has been newly developed. The HIC also has the feature of low power consumption and high RF performance. The developed HIC delivered conversion gain of 20.2dB and noise figure of 4.2dB at supply voltage of 2.7V and dissipation current of 3.7mA in only 5.0mm × 5.0mm×1.0mm size. Power consumption and the size were 60% and 25% of the conventional one, respectively.

The HIC technology will make a great contribution to a highly miniaturized and long time operated mobile communication equipment.

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